What Is Claimed Is:

1. A CMOS process for double vertical channel thin film transistor, comprising the steps of:

forming a gate layer on a substrate;

forming a first insulator layer on the substrate and the gate layer;

forming a semiconductor layer on the first insulator layer, wherein the semiconductor layer has a first area, a second area, and a third area, the third area being formed between the first area and the second area;

forming a first mask on the first area, and implanting N^+ ions to the second area to define a first doped area and a second channel area, and removing the first mask;

forming a second mask on the second area, and implanting P^+ ions to the first area to define a second doped area, a first channel area, and an intrinsic area between the first area and second area, and removing the second mask;

forming a second insulator layer on the first doped area, the second doped area, the first channel area, the second channel area, and the intrinsic area;

exposing the first doped area and the second doped area at the edges of the first insulator layer; and

forming a metal layer on the exposed first doped area and the exposed second doped area.

2. The CMOS process for double vertical channel thin film transistor as claimed in claim 1, wherein the gate layer comprises doped polysilicon, doped amorphous silicon,

transition metals, metal silicide, polycide of metal, aluminum, aluminum alloy, or copper.

3. The CMOS process for double vertical channel thin film transistor as claimed in claim 1, wherein the first insulator layer comprises nitride, oxide, or oxynitride.

4. The CMOS process for double vertical channel thin film transistor as claimed in claim 1, wherein the semiconductor layer comprises single crystal silicon, polysilicon, amorphous silicon, or silicon-germaium.

5. The CMOS process for double vertical channel thin film transistor as claimed in claim 1, wherein the second insulator layer comprises nitride, oxide, and oxynitride.

6. The CMOS process for double vertical channel thin film transistor as claimed in claim 1, wherein the metal layer comprises aluminum, Al-Si alloy, metal silicide, or polycide of metal.

7. A CMOS process for double vertical channel thin film transistor, comprising the steps of:

forming a gate layer on a substrate;

forming a first insulator layer on the substrate and the gate layer;

forming a semiconductor layer on the first insulator layer, wherein the semiconductor layer has a first area, a second area, and a third area, the third area being formed between the first area and the second area;

forming a first mask on the first area, and implanting N^+ ions to the second area to define a first doped area and a second channel area, and removing the first mask;

forming a second mask on the second area, and implanting P^+ ions to the first area to define a second doped area, a first channel area, and an intrinsic area between the first area and second area, and removing the second mask;

forming a second insulator layer covering over the first channel area and the second channel area; and

forming a metal layer on the first doped area, the second doped area, and the intrinsic area.

8. The CMOS process for double vertical channel thin film transistor as claimed in claim 7, wherein the gate layer comprises doped polysilicon, doped amorphous silicon, transition metals, metal silicide, polycide of metal, aluminum, aluminum alloy, or copper.

9. The CMOS process for double vertical channel thin film transistor as claimed in claim 7, wherein the first insulator layer comprises nitride, oxide, or oxynitride.

10. The CMOS process for double vertical channel thin film transistor as claimed in claim 7, wherein the semiconductor layer comprises single crystal silicon, polysilicon, amorphous silicon, or silicon-germaium.

11. The CMOS process for double vertical channel thin film transistor as claimed in claim 7, wherein the second insulator layer comprises nitride, oxide, or oxynitride.

12. The CMOS process for double vertical channel thin film transistor as claimed in claim 7, wherein the metal layer comprises aluminum, Al-Si alloy, metal silicide, or polycide of metal.

13. A CMOS of double vertical channel thin film transistor, comprising:

a gate layer formed on a substrate;

a first insulator layer formed on the substrate and the gate layer, wherein the first insulator layer has a flat part and two vertical walls, the flat part being formed between the two vertical walls;

a semiconductor layer formed on the first insulator layer, wherein the semiconductor layer has two channels formed on the two vertical walls, and a first doped area and a second doped area formed to connect with two ends of the two channels respectively, and an intrinsic area formed on the flat part between the first doped area and the second doped area;

a second insulator layer formed on the semiconductor layer, exposing two sides of the semiconductor layer to form an exposed pattern of the semiconductor layer; and

a metal layer formed on the exposed pattern of the semiconductor layer.

14. The CMOS of double vertical channel thin film transistor as claimed in claim 13, wherein the gate layer comprises doped polysilicon, doped amorphous silicon, transition metals, metal silicide, polycide of metal, aluminum, aluminum alloy, or copper.

15. The CMOS of double vertical channel thin film transistor as claimed in claim 13, wherein the first insulator layer comprises nitride, oxide, or oxynitride.

16. The CMOS of double vertical channel thin film transistor as claimed in claim 13, wherein the semiconductor layer comprises single crystal silicon, polysilicon, amorphous silicon, or silicon-germaium.

17. The CMOS of double vertical channel thin film transistor as claimed in claim 13, wherein the second insulator layer comprises nitride, oxide, or oxynitride.

18. The CMOS of double vertical channel thin film transistor as claimed in claim 13, wherein the metal layer comprises aluminum, Al-Si alloy, metal silicide, or polycide of metal.

19. A CMOS of double vertical channel thin film transistor, comprising:

a gate layer formed on a substrate;

a first insulator layer formed on the substrate and the gate layer, wherein the first insulator layer has a flat part and two vertical walls, the flat part being formed between the two vertical walls;

a semiconductor layer formed on the first insulator layer, wherein the semiconductor layer has two channels formed on the two vertical walls, and a first doped area and a second doped area formed to connect with two ends of the two channels

respectively, and an intrinsic area formed on the flat part between the first doped area and the second doped area;

a second insulator layer formed and covering over the two channels; and

a first, second and third metal layer formed on the semiconductor layer individually.

20. The CMOS of double vertical channel thin film transistor as claimed in claim 19, wherein the gate layer comprises doped polysilicon, doped amorphous silicon, transition metals, metal silicide, polycide of metal, aluminum, aluminum alloy, or copper.

21. The CMOS of double vertical channel thin film transistor as claimed in claim 19, wherein the first insulator layer comprises nitride, oxide, or oxynitride.

22. The CMOS of double vertical channel thin film transistor as claimed in claim 19, wherein the semiconductor layer comprises single crystal silicon, polysilicon, amorphous silicon, or silicon-germaium.

23. The CMOS of double vertical channel thin film transistor as claimed in claim 19, wherein the second insulator layer comprises nitride, oxide, or oxynitride.

24. The CMOS of double vertical channel thin film transistor as claimed in claim 19, wherein the metal layer comprises aluminum, Al-Si alloy, metal silicide, or polycide of metal.